MOHAMMAD KHAVARI TAVANA

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https://scholar.google.com/citations?user=sb3No1YAAAAJ&hl=en

CAREER FOCUS

I am a recent graduate with excellent academic performance. I have a good knowledge about the computer architecture, low power methodology designs at different abstraction layers (application to circuit layers), and modeling memory systems. I am looking for an opportunity that enables me to work with an organization that values motivated new professionals.

WORK EXPERIENCE

PhD Research Fellow
Northeastern University Computer Architecture Research (NUCAR) Laboratory, Boston, Massachusetts, USA
June 2018–current

- Modeling and evaluating data compression algorithms to improve bandwidth and performance of multi-GPU systems
- Implementation and evaluation of row hammer on DDR3 memory modules

Research Assistant (PhD Student)
Northeastern University Computer Architecture Research (NUCAR) Laboratory, Boston, Massachusetts, USA
Sep 2015–May 2018

- Architectural support to enhance energy-efficiency and durability of encrypted non-volatile main memories
- Improving endurance of non-volatile memories using error recovery schemes
- Mitigate disturbance errors in Phase Change Memory using compression and coding techniques

Research Assistant
The Accelerated, Secure, and Energy-Efficient Computing Lab (ASEEC), George Mason University, Fairfax, Virginia, USA *Jan 2014–Aug 2015*

- Dynamic heterogeneous architectures with online phase predication to improve energy-efficiency of computing systems
- Application mapping on many-core systems under process variation to improve reliability and energy consumption
- Energy efficient on-chip power delivery with static and dynamic voltage regulator clustering

PROFESSIONAL SKILLS

Programming

- C/C++, Python, Go, OpenMP, MPI, CUDA, Verilog

Mathematical Analysis tools

- R, Mathematica, Matlab

Hardware Tools

- HSPICE, Synopsys Design Compiler, Xilinx ISE, Simulink

Computer Architecture Modeling and Simulation Tools

- Sniper Multi-core simulator, M-sim and SMTsim (CMP and multi-thread simulator), MICA (a Pin tool for collecting microarchitecture-independent workload characteristics)

Performance Analysis Tools

- Intel VTune, LIKWID, Perf

Server Administration and Consolidation Experience

- Virtualization: VMware ESX, Linux KVM, Xen Cloud Platform (XCP)
- VM management tool: VMware vSphere, Virt Manager

Plotting Tools

- GNUplot, Matplotlib (with python), ggplot2 (with R)

EDUCATION

Ph.D., Computer Engineering
Northeastern University, Boston, Massachusetts, USA *Sep 2015–May 2018*
GPA: 3.77/4
Thesis: Architectural support for designing dependable non-volatile main memories

Ph.D., Computer Engineering (*transferred*)
George Mason University, Fairfax, Virginia, USA *Jan 2014–Aug 2015*

Master of Science, Computer Engineering
Sharif University of Technology, Tehran, Iran *Sep 2008–Jan 2011*
GPA: 17.23/20
Thesis: Low-overhead checkpointing for real-time and fault-tolerant systems

Bachelor of Science, Computer Engineering
Islamic Azad University, South Branch, Tehran, Iran *Sep 2004–Aug 2008*
GPA: 16.90/20
Thesis: Design and implementation of multi-purpose wireless sensor nodes with RFM12 module and AVR microcontroller

HONORS/AWARDS

- Outstanding Graduate Research Award, College of Engineering at Northeastern University, 2018
- Chair's Scholarship at Northeastern University
- ICCD 2017 Best Paper Award
- Graduate Research Assistantship from Northeastern University (Spring 2017, Summer 2017, and Fall 2017)
- Provost Scholarship at George Mason University (Fall 2014, Spring 2015, Summer 2015)
- Graduate Research Assistantship at George Mason University (Spring 2014, Summer 2014)
- DAC Richard Newton Young Student Fellow Award 2014
- DSD 2012 Best Paper Nomination

MEMBERSHIP

- IEEE Student Member
- ACM Student Member
- ACM SIGARCH, and ACM SIGDA group member
- Member of the Northeastern University Computer Architecture Research (NUCAR) Laboratory (Jan 2016-Current)
- Member of the Embedded Systems Laboratory (ESL) at Northeastern University (Sep 2016, Jan 2016)
- Member of the Accelerated, Secure, and Energy-Efficient Computing Lab (ASEEC) at George Mason University (Jan 2014-Aug 2015)
- Member of the Embedded Systems Research Laboratory (ESRLab) at Sharif University of Technology (Sep 2009-Jan2011)

PUBLICATIONS

- **JournalArticles**

1. Mohammad Khavari Tavana, Amir Kavyan Ziabari, David Kaeli, "Block Cooperation: Advancing Lifetime of Resistive Memories by Increasing Utilization of Error Correcting Codes", ACM Transactions on Architecture and Code Optimization (TACO), In press. **TACO(2018)**

2. Mohammad Khavari Tavana, Yunsi Fei, David Kaeli, "Nacre: Durable, Secure and Energy-efficient Non-Volatile Memory Utilizing Data Versioning", IEEE International Conference on Computer Design (**ICCD**), 2017. **Best paper Award**. This paper is selected for publishing in IEEE Transactions on Emerging Topics in Computing (**TETC**) journal. **TETC(2018)**

3. Mohammad Khavari Tavana, et al., "ElasticCore: A Dynamic Heterogeneous Platform with Joint Core and Voltage/Frequency Scaling", IEEE Trans. VLSI Syst., 26(2), 2018. **TVLSI(2018)**

4. Mohammad Hossein Hajkazemi, Mohammad Khavari Tavana, Tinoosh Mohsenin, Houman Homayoun, "Heterogeneous HMC+DDRx Memory Management for Performance-Temperature Trade-offs", ACM Journal on Emerging Technologies in Computing Systems, 14(1), 2017. **JETC(2017)**

5. Mohammad Salehi, Mohammad Khavari Tavana, Semeen Rehman, Muhammad Shafique, Alireza Ejlali, Jrg Henkel, "Two-State Checkpointing for Energy-Efficient Fault Tolerance in Hard Real-Time Systems", IEEE Trans. VLSI Syst. 24(7), 2016. **TVLSI(2016)**

6. Mohammad Khavari Tavana, et al., "Dynamically Adaptive Register File Architecture for Energy Reduction in Embedded Processors", Elsevier Microprocessors and Microsystems, 39(2), 2015. **Elsevier Microprocessors and Microsystems(2015)**

7. Mohammad Khavari Tavana, et al., "Simultaneous Hardware and Time Redundancy with Online Task Scheduling for Low Energy Highly Reliable Standby-Sparing System", ACM Transactions on Embedded Computing Systems, 13(4), 86, 2014. **TECS(2014)**

- **ConferencePapers**

1. Mohammad Khavari Tavana, Amir Kavyan Ziabari, Mohammad Arjomand, Mahmut Kandemir, Chita Das, David Kaeli, "REMAP: A Reliability/Endurance Mechanism for Advancing PCM", ACM International Symposium on Memory Systems, 2017. **MEMESYS(2017)**.

2. Mohammad Khavari Tavana, David Kaeli, "Cost-Effective Write Disturbance Mitigation Techniques for Advancing PCM Density", IEEE/ACM International Conference on Computer-Aided Design, 2017. **ICCAD(2017)**

3. Amin Jadidi, Mohammad Arjomand, Mohammad Khavari Tavana, David Kaeli, Chita Das, Mahmut Kandemir, "Exploring the Potential for Collaborative Data Compression and Hard-Error Tolerance in Resistive Memories", IEEE/IFIP International Conference on Dependable Systems and Networks, 2017. **DSN(2017)**

4. Mohammad Khavari Tavana, Amir Kavyan Ziabari, David Kaeli, "Live Together or Die Alone: Block Cooperation to Extend Lifetime of Resistive Memories", IEEE Design, Automation and Test in Europe, 2017. **DATE(2017)**

5. Divya Pathak, Mohammad Hossein Hajkazemi, Mohammad Khavari Tavana, Houman Homayoun, Ioannis Savidis, "Load Balanced On-Chip Power Delivery for Average Current Demand", ACM Great Lakes Symposium on VLSI, 439-444, 2016. **GLSVLSI(2016)**

6. Divya Pathak, Mohammad Hossein Hajkazemi, Mohammad Khavari Tavana, Houman Homayoun, Ioannis Savidis, "Energy efficient on-chip power delivery with run-time voltage regulator clustering", IEEE International Symposium on Circuits and Systems, 1210-1213, 2016. **ISCAS(2016)**

7. Mohammad Khavari Tavana, Mohammad Hossein Hajkazemi, Divya Pathak, Ioannis Savidis, Houman Homayoun, "ElasticCore: Enabling Dynamic Heterogeneity With Joint Core and Voltage/Frequency Scaling", ACM/EDAC/IEEE Design Automation Conference, 151:1-151:6, 2015 **DAC(2015)**

8. Mohammad Salehi, Muhammad Shafique, Florian Kriebel, Semeen Rehman, Mohammad Khavari Tavana, Alireza Ejlali, Jorg Henkel, "dsReliM: Power-constrained reliability management in Dark-Silicon many-core chips under process variations", International Conference on Hardware/Software Codesign and System Synthesis, 75-82, 2015. **CODESS+ISSS(2015)**

9. Mohammad Hossein Hajkazemi, Michael Chorney, Reyhaneh Jabbarvand Behrouz, Mohammad Khavari Tavana, Houman Homayoun, "Adaptive Bandwidth Management for Performance-Temperature Trade-offs in Heterogeneous HMC+DDRx Memory", ACM Great Lakes Symposium on VLSI, 391-396, 2015. **GLSVLSI(2015)**
10. Mohammad Khavari Tavana, Divya Pathak, Mohammad Hossein Hajkazemi, Maria Malik, Ioannis Savidis, Houman Homayoun, "Realizing complexity-effective on-chip power delivery for many-core platforms by exploiting optimized mapping", IEEE International Conference on Computer Design, 581-588, 2015. **ICCD(2015)**
11. Mohammad Hossein Hajkazemi, Mohammad Khavari Tavana, Houman Homayoun,"Wide I/O or LPDDR? Exploration and analysis of performance, power and temperature trade-offs of emerging DRAM technologies in embedded MPSoCs", IEEE International Conference on Computer Design, 62-69, 2015. **ICCD(2015)**
12. Mohammad Salehi, Mohammad Khavari Tavana, Semeen Rehman, Florian Kriebel, Muhammad Shafique, Alireza Ejlali, Jorg Henkel,"DRVS: Power-efficient reliability management through Dynamic Redundancy and Voltage Scaling under variations", ACM/IEEE International Symposium on Low Power Electronics and Design, 225-230, 2015. **ISLPED(2015)**
13. Vasileios Kontorinis, Mohammad Khavari Tavana, et al., "Enabling Dynamic Heterogeneity Through Core-on-Core Stacking", ACM/EDAC/IEEE Design Automation Conference, 1-6, 2014. **DAC(2014)**
14. Mohammad Khavari Tavana, et al. "Energy-efficient Mapping of Biomedical Applications on Domain-Specific Accelerator under Process Variation", ACM/IEEE International Symposium on Low Power Electronics and Design, 275-278, 2014. **ISLPED(2014)**
15. Meisam Abdollahi, Mohammad Khavari Tavana, et al. "ONC3: All-Optical NoC Based on Cube-Connected Cycles with Quasi-DOR Algorithm", IEEE Euromicro Conference on Digital System Design, 296-303, 2012. **Best Paper Nomination - DSD(2012)**
16. Mohammad Khavari Tavana, et al., "Feedback-Based Energy Management in a Standby-Sparing Scheme for Hard Real-Time Systems", IEEE Real-Time Systems Symposium, 349-356, 2011. **RTSS(2011)**

WORK-IN-PROGRESS PRESENTATION

- Mohammad Khavari Tavana, et al., "Energy-Efficient Mapping of Real-time Tasks in Many-core Accelerator under Process Variation", ACM/EDAC/IEEE Design Automation Conference (DAC), Presented in work-in-progress(WIP) session, 2014. **DAC(2014)**

TEACHING EXPERIENCE

- Instructor, Embedded Design: Enabling Robotics (Northeastern University, Fall 2016)
- Teacher Assistant, Green Computing (Sharif University of Technology, Fall 2011)
- Teacher Assistant, Digital system design lab (Sharif University of Technology, Spring 2010)

SERVICES

Reviewer of the ACM Transactions on Architecture and Code Optimization (TACO) *2018*
Reviewer of the Journal of Circuits, Systems, and Computers (JCSC) *2018*
Reviewer of the 33nd IEEE International Conference on Computer Design. ICCD *2015*
Reviewer of the 25th Great Lake Symposium on VLSI. GLSVLSI *2015*
Reviewer of the 32nd IEEE International Conference on Computer Design. ICCD *2014*
Reviewer of the 24th Great Lake Symposium on VLSI. GLSVLSI *2014*
Reviewer of the IEEE International Symposium on Quality Electronic Design. ISQED *2014*
Reviewer of the Fourth International Green Computing Conference, IGCC *2013*
Technical Program Committee (TPC) The International Conference on Smart Energy Systems (SES), *2019*
Technical Program Committee (TPC) of 6th Asia Symposium on Quality Electronic Design. ASQED *2015*

REFERENCES

Dr. David Kaeli (**advisor**)	kaeli@ece.neu.edu	http://www.ece.neu.edu/fac-ece/kaeli.html
Dr. Yunsi Fei	yfei@ece.neu.edu	http://www.ece.neu.edu/people/fei-yunsi
Dr. Houman Homayoun	hhomayou@gmu.edu	https://ece.gmu.edu/~hhomayou/