An All-digital Receiver for Low Power, Low Bit-rate Applications using Simultaneous Wireless Information and Power Transmission

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***Abstract*—Wireless RF power transmission is emerging as a promising approach to enable battery-less wireless networked sensor systems. However, when data communication and RF energy recharging occur in-band, sharing the RF medium raises architectural and protocol level challenges. To avoid the tradeoffs of alternating between energy and data communication, Simultaneous Wireless Information and Power Transmission (SWIPT) has been proposed as a feasible solution to enable joint power and data transfer. Different from existing approaches, where the incident energy is split between decoding and harvesting blocks at the receiver chain, this paper describes the design and implementation of an all-digital receiver circuit by leveraging the internal control signals of the circuit, targeting ultra-low power consumption, low bit-rate applications in SWIPT. A proof-of-concept receiver is modeled, implemented using off-the-shelf hardware, and validated through extensive experiments. Quantitative results demonstrate the benefits of this joint energy-data reception approach through a single receiver chain, offering bit-rates of 400 bps in the considered set-up.**

I. Introduction

Wireless networked sensing systems are the "invisible" enablers of the Internet of Things [1]. Powering these systems is becoming the crucial challenge, as key requirements such as cost effectiveness and very small form factors are difficult to meet by using nodes that have low-capacity batteries [2].

Recent advances towards powering and/or recharging these systems concerns the use of dedicated Energy Transmitters (ETs) that send RF power to the system nodes wirelessly [3]. Using the RF spectrum for both energy and data transfer, however, may seriously affect network operation as the high power energy alters the data signal amplitude. Therefore, devising methods for energy provisioning without affecting data communications is a key challenge currently being tackled by the research community [4]. In this context, transmission of both point-to-point energy and concurrent enabling of downlink communications from a base station (BS) to a node has been referred as Simultaneous Wireless Information and Power Transmission (SWIPT) [5]. This approach has shown remarkable benefits, since the signal receiver can be integrated in the energy harvester [6].

High-efficient energy harvesters integrate switch-mode DC-DC converters to optimize the operation of the rectifying stage [7], [8]. Their operation is based on harvesting an amount of energy and temporarily storing it in a low-leakage small capacitor. Once enough energy has been harvested, this is transferred in a form of a high amplitude, short time-scale energy pulse to the energy storage unit. Unfortunately, the non-linear packetization of the energy modifies the received waveform, hence making it difficult to integrate classical approaches for data reception in the energy harvester, such as the one presented in [6].

This paper presents an all-digital receiver architecture for low-bit-rate, ultra-low-power applications, where the digital signal used to control the switch-mode operation of the energy harvester is opportunistically employed to allow signal reception through a digital counter. The key idea here is to leverage the period of the control signal to estimate the received information bit, by counting the number of times the current spikes are injected by the circuit. We base this approach on our experimental finding that the number of spikes per unit time is input power dependent.

As an important contribution, we demonstrate through our experimental testbed that the communicating sensor can successfully decode information at a rate of 400 bps using a software-based approach that can be integrated into the programmed routines of the microprocessor connected to the RF energy harvesting circuit. Thus, our approach can entirely eliminate dedicated hardware for signal detection.

The rest of the paper is organized as follows. In Section II we describe the fundamentals of SWIPT and model the all-digital receiver. Section III validates the presented model and evaluates the performance of this approach. Finally, Section IV concludes the paper.

II. Operation Principle

In this section we briefly revise the fundamentals of SWIPT [5] and define the concept of joint energy and data transmission. Then, we present the operational principle of the

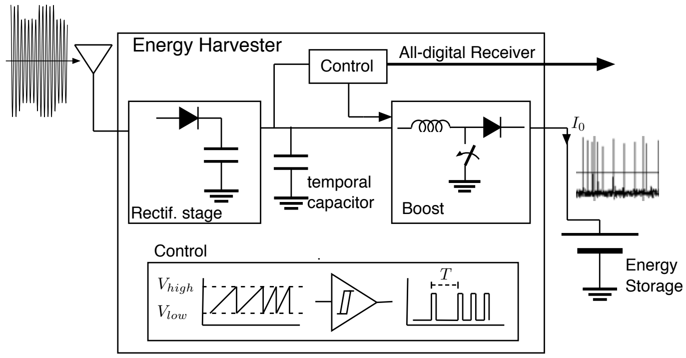

Fig. 1. Internal operation of an energy harvester equipped with a DC-DC boost converter. The time between activations of the control unit is inversely related to the harvested power.

all-digital data receiver integrated with high-efficient, switch-mode RF energy harvesters.

A. SWIPT Transmitted Signal

The ET (or base station) propagates a powerful RF wave, with incident average power P_H at the antenna of the recipient node, which the latter harvests to recharge its battery. In order to transmit information, the ET modulates the envelope of the RF wave employing a pulse energy modulation [6]. Accordingly, we define the required power to transmit a logical '1' and '0' as P_1 and P_0, respectively, such that:

$$P_H = \frac{1}{2}(P_1 + P_0). \tag{1}$$

To measure the amount of energy that is being devoted to effectively modulate the information, we employ the modulation depth index, defined as:

$$h = \frac{P_1 - P_0}{P_1 + P_0}, \tag{2}$$

such that if $h = 1$ the transmission of a logical '0' is done through silence, whereas for $h < 1$, the allocated power in P_0 accomplishes $P_0 < P_1$.

Due to the governmental regulations, the transmitted power from the ETs is limited, hence limiting the maximum transmission range of the ETs. For e.g., the FCC permits a maximum of 4W emission of isotropic radiation. We assigning the maximum allowed power to the transmission of the logical '1'. The proposed design brings a rate-energy trade-off in the transmission of simultaneous energy and data. At a high level, transmitting with higher modulation depths, with fixed P_1, yields to higher bit-rates, whereas it reduces the average harvested power, P_H.

B. Energy Harvester

The considered energy harvester in this work integrates two separated and generic stages for energy optimization [7]. First, a rectifying circuit is employed that can convert with very high efficiency the harvested power. Then, a DC-DC boost converter operating in discontinuous conduction mode (DCM) is considered to transfer the accumulated energy in a temporal capacitor towards the energy storage unit (i.e., a super-capacitor or battery). The control unit handles the operation of this converter. The configuration of the considered energy harvester topology is described in Fig. 1.

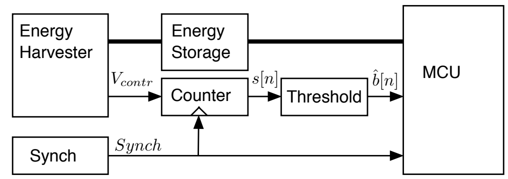

Fig. 2. Block diagram of the integrated, all-digital receiver for SWIPT. It is based on counting the number of activations of the energy harvester control signal.

The aim of this dual-stage design is to optimize the transfer of energy by accurately matching the input impedance of the rectifying stage, which depends on its output load [9]. In particular, when connecting a rectifying stage for energy harvesting applications to an energy buffer, it shows a time-variable conversion efficiency, showing poor performance when the output capacitor voltage is either too low or too high [7]. For this, a small capacitor is connected to the output of the rectifier, which permits to rapidly skip the low-voltage operation regime (i.e., below V_{low} voltage level). When its output voltage surpasses a given threshold, V_{high}, the stored energy is high efficiently transferred to the output energy buffer through a DC-DC boost converter, leaving the voltage at the temporal capacitor at V_{low} voltage (the duration time of this action is referred as *on-time*). As such, we observe that the voltage of the temporal capacitor V_{cap} approximates a sawtooth waveform [8], and the output current of the energy harvester is in form of short time-scale spikes. The operation of a dual-stage energy harvester is described in Fig. 1

We see that the period T of the sawtooth waveform depends on the input power. In particular, the energy that is transferred each *on-time* is given by:

$$\Delta E = \frac{1}{2} C_{cap} \left(V_{high}^2 - V_{low}^2 \right), \tag{3}$$

where C_{cap} refers to the capacitance of the temporal capacitor. During the steady-state operation of the energy harvesting and neglecting the leakage current of the capacitor, the ΔE energy that is transferred to the output load equals to the energy that has been stored in the capacitor during the last period T. Both V_{high} and V_{low} are set as a design parameters to optimize the harvesting process, and we can assume that the energy during that time is harvested with optimal and constant efficiency, η. Hence:

$$\Delta E = \eta P_H T \tag{4}$$

where P_H stands for the harvested power. Therefore, the period of the sawtooth depends on the input power as:

$$T = \frac{1}{2\eta P_H} C_{cap} \left(V_{high}^2 - V_{low}^2 \right). \tag{5}$$

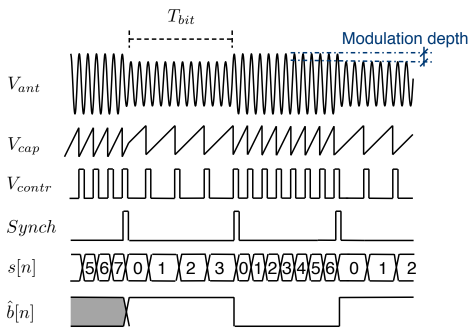

Fig. 3. Internal operation waveforms of the all-digital receiver.

The selection of the capacitor value will define the eventual efficiency of the energy harvester, as well as the achievable data rate of the receiver. Particularly, large values will increase the period time, hence reducing the eventual data-rate. On the contrary, reducing it will increase the switching times and reduce the ΔE, hence potentially making the process less energy efficient.

C. All-digital Receiver

The architecture of the all-digital receiver is shown in Fig. 2. It is composed of three separate units, namely a counter, a threshold comparator and a synchronization unit. The all-digital receiver leverages the control signal of the energy harvester that activates the DC-DC boost converter stage to estimate the power of the given symbol. To do this, the receiver simply counts the number of times that the control signal has been activated during the reception of a given bit, T_{bit}. The timing is provided by the synchronization unit. Afterwards, the number of counts is compared to a threshold that decides whether the received symbol is a one or a zero. The synchronization unit aims to determine the optimal sampling point. For this, similar digital-based approaches as in [10] can be implemented. In order to determine the appropriate timing and the threshold for comparison, a preamble sequence needs to be transmitted prior the transmission of the information.

Fig. 3 describes the logical operation of the all-digital receiver. In the figure, we show the received signal at the antenna V_{ant}. This signal is harvested through the rectifying stage of the energy harvester and its power is transferred to the temporal capacitor. The control unit of the energy harvester activates the DC-DC boost converter through V_{contr}, which rapidly discharges the temporal capacitor and showing a sawtooth signal in V_{cap}. This control signal V_{contr} is also used to estimate the power of the symbol in the all-digital receiver. In particular, the output of the counter unit, $s[n]$ shows the number of times that the control signal has been activated during a T_{bit} time. According to the depicted example, during the reception of a symbol '0', V_{contr} has been activated 3 times, whereas it has been activated 6 times to represent the symbol '1'.

Provided that the period of the control signal is independent of T_{bit}, the number of times that the control signal becomes active during T_{bit} is variable, even in a noise-free environment.

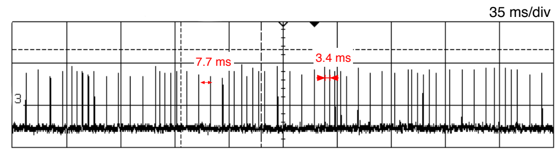

Fig. 4. Experimentally sensed output current of the energy harvester when receiving an input signal with powers $P_0 = -9$ dBm and $P_1 = -6$ dBm.

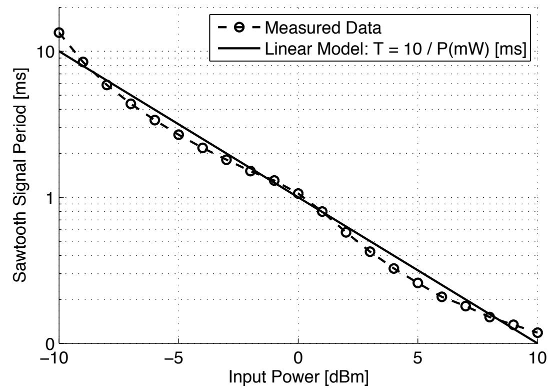

Fig. 5. Input power dependence of the period of the control signal. Comparison between predicted model and actual operation.

In order to successfully receive information, we must guarantee that the number of control pulses during the reception of a '0', in the worst case, needs to be lower than the number of pulses during the reception of a '1' in the worst case. As such, T_{bit} is constrained such that the following condition is guaranteed:

$$\left\lceil \frac{T_{bit}}{T_0} \right\rceil < \left\lfloor \frac{T_{bit}}{T_1} \right\rfloor, \tag{6}$$

where T_0 and T_1 refer to the period of the control signal during the transmission of a logical '0' and a logical '1', respectively, and $\lceil \cdot \rceil$ and $\lfloor \cdot \rfloor$ refer to the ceil and floor functions, respectively.

Given the simplicity of this approach, sensors can implement a software-based all-digital receiver that is run in a basic micro-controller connected to the harvesting circuit, thus reducing significant hardware size, complexity, cost and power consumption.

III. Performance Evaluation

In this section we demonstrate the feasibility of this approach and evaluate the performance of an all-digital data receiver.

A. Off-the-shelf Energy Harvester

We first characterize an off-the-shelf energy harvester to be used as a signal receiver. For this, we have considered the Powerharvester P2100 from Powercast Co [8]. This energy harvester implements a DC-DC boost converter to maximize the energy transfer. Due to the fact that it is an integrated circuit, we do not have access to its internal signaling. Accordingly, we have measured the output current of this circuit to determine the required signals, since the output current is only active when during the *on-time* of the DC-DC boost converter.

Fig. 4 shows the output current of the energy harvester, with $P_0 = -9$ dBm and $P_1 = -6$ dBm, $C_{cap} = 10\ \mu$F and an output capacitor of 220 mF for energy storage. As it is shown, the variation of the input power effectively modulates the period of the generated spikes at the output current, showing a period of 7.7 ms and 3.4 ms for P_0 and P_1, respectively.

We then show in Fig. 5 the relation between the input power at the energy harvester and the period of the control signal (and, hence, the period of the current spikes). As it is shown, the predicted behavior of this period in (5) is consistent with the obtained results, showing that, with our considered circuit values, the period can be approximated by: $T[\text{ms}] \approx 10/P[\text{mW}]$. The observed mismatch between curves is due to the dependence of the efficiency with the input power, as reported in [11].

B. Rate-Energy Trade-off

Given that the maximum allowed transmitting power is constrained by external regulation, a trade-off between achievable rate and transferred energy appears. That is, the transmission of the logical '1' is set to the maximum power, whereas the modulation depth will determine the allocated power of the logical '0'. Low values of modulation depth maximizes the energy transfer, since the average power P_H is larger. However, this reduces the distance between symbols, hence requiring longer T_{bit} times to detect a significant difference at the output of the digital counter, $s[n]$.

We have evaluated the maximum bit-rate that can be achieved by following this approach. For this, we have calculated the minimum T_{bit} that be utilized at given input powers P_1 and P_0, such that it is certain that the number of control actions detected during this the reception of a logical '0' is smaller than the number of actions of a logical '1'. To bound this bit rate, we have considered a fully-synchronized, noise-free environment, such that this is constrained by the internal limitations of our approach.

We show in Fig. 6 the maximum achievable bit-rate as a function of the modulation depth index, for different values of P_1. These set of values aim to evaluate the maximum bit rate at a different distance between transmitter and receiver. As it can be observed, higher values of the index between, achieve higher bit-rates, reaching up to 422 bps with an index $h = 0$ and $P_1 = 10$ mW, that is the total harvested power equals to 5 mW. Alternatively, we show that as this ratio increases, the maximum bit-rate rapidly drops. In particular, we observe that the bit-rate significantly drops for all values of input powers for modulation depth indices below $h < 0.1$.

IV. Conclusions

We introduced an opportunistic all-digital receiver for simultaneous wireless and information power transmission (SWIPT) with highly-efficient, switch-mode RF energy harvesters. We showed that the overlapped data transmission can be easily recovered by simply monitoring the internal control signals of an energy harvester. This approach enables a software-based data reception with its associated benefits. Among others, no separate data reception hardware is required, thus reducing manufacturing cost and size, as well as promises a potential reduction in power consumption. To validate this approach, we have modeled and implemented a proof-of-concept receiver, based on current off-the-shelf hardware to successful data reception rates of over 400 bps. We believe our design will impact future joint energy and data RF harvesters by enabling higher decoding bit-rates, while still meeting the desired performance over the power processing stage.

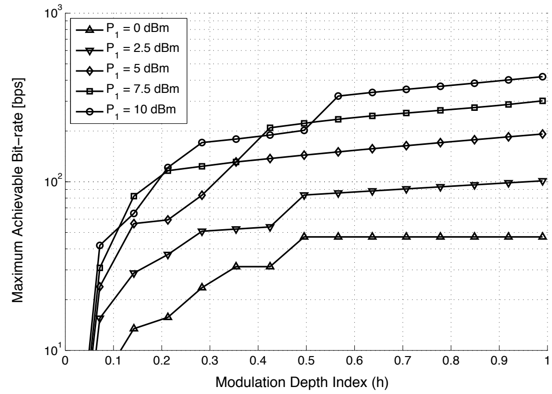

Fig. 6. Rate-energy trade-off of the proposed software-based receiver approach for SWIPT applications.

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