Computationally Efficient Look-up-Tables for Behavioral Modelling and Digital Pre-distortion of Multi-Standard Wireless Systems

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Abstract. Wireless systems such as cellular networks have begun to see proposals for increased operational flexibility through reuse of the same hardware but with different signal standards. This paper presents an approach to characterise a power amplifier (PA) for multiple signal standards. Following from this, behavioural modeling demonstrates that the same coefficients trained for a single signal standard can be effectively applied to multiple signal standards. This result is used to design and implement a digital predistorter (DPD) capable of linearizing for different signal standards on a Field Programmable Gate Array (FPGA). This implementation is experimentally validated on a state-of-the-art RFSoC FPGA from Xilinx to correct for PA non-linearities in the transmit chain using an efficient hardware design. Additionally the behavioural modelling and DPD solutions have been validated using distinctly different PAs to demonstrate the proposed look up table approach is hardware agnostic and works when the appropriate dimensions are set for the dynamic nonlinear structure in each case.

Keywords: Behavioural modeling · Pre-distortion · Memory Polynomial · Software Defined Radio · FPGA.

1 Introduction

Software Defined Radio (SDR) has been around for several decades, but the implementations of such radios, despite including reconfigurable elements such as Field Programmable Gate Arrays (FPGAs), are surprisingly static. Most SDRs are configured to support one protocol and a specific design, once deployed, is seldom changed. In previous work, researchers have addressed the issue by demonstrating the reception of multiple different protocols with the same front end [11], [18]. In this paper, we address the issue of handling multiple different signal standards on the transmit side. The transmitter makes use of a power amplifier (PA) and, to obtain maximum power efficiency, the PA is operated

near its saturation point, which leads to nonlinear distortion as well as significant memory effects.

Pre-distortion or linearization of signals to compensate for the non-linearity and memory effects of power amplifiers (PAs) is a broad area of research in telecommunication systems [24, 17, 2]. The trend for linearization algorithms is to apply increasingly complicated nonlinear structures such as artificial neural networks [12] or vector-switched Volterra series [1] in order to pre-distort the input signal. The nonlinear pre-distorter structures contain weights which must be trained and it is this training operation that introduces the highest computational cost. Look-up tables have been implemented in the past to provide coefficients for the pre-distorter [22], however these solutions have not previously been applied for use with multi-standard radios. A compelling objective for modeling these systems is to identify the most computationally efficient structure which can accurately characterise the PA behaviour and estimate the output signal. A structure that encompasses memory effects, various bandwidths and nonlinearity is the Volterra series, however the number of coefficients used in a Volterra series increases rapidly with increasing nonlinear order or memory depth. More compact memory models can be achieved using the memory polynomial and generalised memory polynomial.

A limitation associated with behavioural modeling of power amplifiers has been that a model trained with one standard of input and output signals is not typically applicable to other signal standards, and thus the resulting behavioural models are traditionally limited to a single protocol. This is in direct contravention to the ethos expected of a software defined radio. Ideally the radio should be capable of transmitting multiple standards; in this research we focus on 3G, 4G and 5G cellular network communications. Wideband Code Division Multiple Access (WCDMA) is widely used in 3G networks [16], while Orthogonal Frequency-Division Multiplexing (OFDM) is utilised in 4G and 5G networks. 5G offers a wider range of configurations for the construction of signals and as a result different signal formats can be generated compared to 4G. In this paper we propose a strategy to model the behaviour of the PA such that the necessary coefficients can be used across these different signal modulation schemes. This structure is then extended to the practical case of providing a digital Pre-Distorter (DPD). The contribution of this paper is describing how the same trained model or DPD coefficients to be used across different signal standards. The result is a look-up-table (LUT) based DPD implementation for multi-standard cognitive radios. The DPD is implemented on a state-of the-art Xilinx RFSoC FPGA which integrates an embedded ARM processor, FPGA fabric, and RF frontend in a single package. In this paper LUT refers to the storage of coefficients for the DPD implementation and not the look up tables that are part of the FPGA fabric.

In Section 2 we introduce the background information about power amplifier non-linearity, behavioural modeling, and related work. The two main areas for validation of this work cover behavioural modelling and DPD. In both cases experimentally measured results for power amplifier operation with different input

signal standards are collected as described in Sec. 3.1. From these measurements, power level matching between standards can be achieved and the corresponding sets of coefficients applied to different standards, first for behavioural modelling as described in Sec. 3, and next for predistortion as described in Sec. 4. Results of the DPD experiments using signals from different signal standards are presented in Sec. 5. Conclusions from this work are summarised in Sec. 6.

2 Background

2.1 Nonlinear Power Amplifiers with Memory Effects

Power amplifiers perform a critical function in wireless communication systems, which is to transfer the supplied power to a modulated signal at high frequency in order to transmit it over greater distances. Unfortunately, in order to operate the power conversion of the power amplifier efficiently, the resulting PA output signal suffers distortion in the form of dynamic and non-linear behaviours. In particular, Gallium Nitride (GaN) power amplifiers have become the technology of choice for high power applications such as cellular network basestations and satellite communications. This is as a result of GaN devices having a higher breakdown field allowing them to operate at higher output voltages compared to other semiconductor substrates. Additionally electrons on GaN have a higher saturation velocity and large charge capability which allow high current density. GaN devices however demonstrate non-linear behaviour when operated in efficient modes and can experience charge trapping which is more difficult to characterise than for other semiconductor technologies. GaN PAs may be modelled using non-linear digital filters with sufficient order of nonlinearity and number of memory taps.

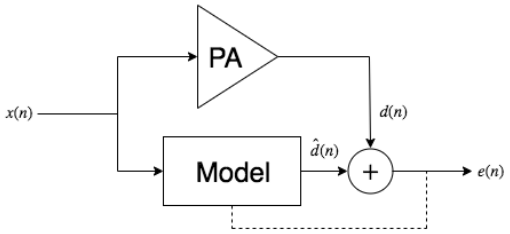

Fig. 1. PA model training

The operation of a digital filter is to take input signal samples x(n), combine the current sample and previous samples, weight all of them and sum the resulting products. A nonlinear filter contains weights H(n), which are multiplied by various combinations of the input samples. The objective is for the output $\hat{d}(n)$ to be comparable to the desired output signal d(n). The operation of training

these nonlinear filter or model coefficients, is done in such a way as to minimise the difference between $d(n)$ and $\hat{d}(n)$. Fig. 1 depicts this relationship.

2.2 Discrete Dynamic Nonlinear Models and Training Algorithm

For this research, Least Squares (LS) was chosen as the coefficient training technique with the following behavioural models : memory polynomial (MP) and generalised memory polynomial (GMP).

Parameter estimation or training of the behavioural model is as important as the capabilities of the model chosen. Least squares estimation is a direct estimation process where the input and output signals are analysed in vector form and an optimal solution can be derived from direct matrix inversion [15]. The least squares solution can be extracted solely with the input and output sample data. The least squares algorithm chooses weights to minimise the function in Eq. 1.

$$J(N) = \frac{1}{N}\sum_{t=1}^{N}(y(t) - X^T(t)\vec{w}) \tag{1}$$

Where N represents the length of the signal data sets, X and y denote the input and output signal datasets respectively. $\vec{w}$ refers to the calculated weights.

A range of behavioural models were considered for this work. The main difference between them stems from the different number of coefficients used in each to perform behavioural modeling. These models can be classified as subsets of the Volterra model, for which the discrete version is given by Eq. 2. The Volterra model is ideally suited for characterizing nonlinear systems with memory effects such as power amplifiers.

$$y_{VS}(n) = \sum_{i_1=0}^{M-1}\cdots\sum_{i_P=0}^{M-1} h_p(i_1,\cdots,i_p)\prod_{i=1}^{P} x(n-i_r) \tag{2}$$

Here $x(n)$ and $y(n)$ are the input and output signals to the power amplifier respectively. $h_p(i_1, ..., ip)$ represents the filter co-efficient expansion utilising P, the highest order for the non-linearity of the Volterra series expansion. M represents the maximum memory depth.

The memory polynomial is a model derived from the Volterra model comprised only of the linear terms and higher order products with the same time-shifts [7]. Combining these higher order products of delayed input signal components into a single array, form the memory polynomial as described by Eq. 3. While the model only considers a fraction of the input signal combinations present in the Volterra series, the addition of delayed input samples allow the characteristic memory effect of the power amplifier to be modelled.

$$y_{MP}(n) = \sum_{p=1}^{P}\sum_{m=0}^{M} a_{pm}x(n-m)|x(n-m)|^{p-1} \tag{3}$$

where a_{pm} are the estimated model parameters, and P and M represent the highest non linear order and the memory depth of the model, respectively.

The GMP [20] can be considered as taking multiple delayed MP models, given by Eq. 3, to include leading and lagging cross-terms as seen in Eq. 4. In this way a wider range of combinations of delayed input signal samples from the Volterra model are considered compared to the memory polynomial.

$$\begin{aligned} y_{GMP}(n) = & \sum_{k\epsilon K_a} \sum_{l\epsilon L_a} a_{kl} x(n-l)|x(n-l)|^k + \\ & \sum_{k\epsilon K_b} \sum_{l\epsilon L_b} \sum_{m\epsilon M_b} b_{klm} x(n-l)|x(n-l-m)|^k + \\ & \sum_{k\epsilon K_c} \sum_{l\epsilon L_c} \sum_{m\epsilon M_c} c_{klm} x(n-l)|x(n-l+m)|^k \end{aligned} \tag{4}$$

Here K_a and L_a index the arrays for the input signal and its envelope; K_b,L_b and M_b refer to the indexing of the input signal and its lagging envelope; and K_c,L_c and M_c are index arrays for the input signal and its leading envelope. a_{kl}, b_{klm} and c_{klm} are the estimated model parameters.

The Normalised Mean Square Error (NMSE) denotes a common figure of merit used to indicate the accuracy of a model in characterising power amplifiers behaviour [13]. The NMSE is convenient as it only requires a single value to describe the overall deviations between predicted and measured values of the model output $\hat{d}(n)$ and experimentally validated output $d(n)$ over what can be large datasets.

2.3 Related Work

Look-up-table (LUT) solutions for nonlinear power amplifiers have been previously introduced for both behavioural modelling and predistortion. The chronology of these LUT solutions shows new methods have emerged for both applications.

As a means of modeling the behavior of RF power amplifiers, a number of different LUT approaches have been proven to be effective. A data-based nested LUT structure has equivalent performance to the memory polynomial for modeling of power amplifiers exhibiting memory effects as shown in [9]. This LUT approach has been further extended to a 2-D LUT model for transmitters/PAs exhibiting memory effects. With an additional dimension [10], the LUT is expanded to take into account the dependency of the device behavior on the preceding samples. The 2-D LUT models the transfer function of the device under test as a complex gain that is a function of the magnitude of the current and previous samples. More recently, Nunes et al. have demonstrated a LUT solution for high efficiency power amplifier architecture [23]. A newer class of power amplifier behavioral model named hybrid look-up tables (H-LUT) improves the performance of a conventional nested LUT model [6]. Here, a combination of a memoryless LUT and nested LUT are connected in parallel. The accuracy of

the proposed model is also better suited for being trained with smaller training datasets compared to the nested LUT model alone.

In [4] a LUT is pre-trained for a power amplifier and used to pre-distort the signal supplied to the PA. At that time, the pretrained LUT demonstrated a solution requiring four orders of magnitude less memory, three orders of magnitude reduction in convergence time and eliminated the reconvergence time needed following a channel switch. FPGA-based LUT solutions have been proposed for switchmode PAs [5]. As a case study a polar configured Class F switch-mode PA is shown to be effectively linearized by the proposed approach. Additional enhancements to the LUT implementation have been proposed [8] [21]. Here the aim is to reduce the hardware resources required to implement the solution in an FPGA. Savings of total hardware resources can be made in terms of arithmetic hardware blocks though the structure of the DPD calculations are re-ordered. Molina et. al. [19] show how a predistorter with lower complexity than polynomial models translated to a LUT. This is achieved by expressing a DPD function as a system of linear-in-parameter equations. Least squares is used to train the LUT coefficients directly. More recent work on LUT [3] is based on spline-interpolated look-up-tables. While similar to established polynomial-based solutions, a reduction in DPD processing is presented. The use of LUT predistorters has been adopted for optical communications also. Implementations for nonlinear weighted look-up-table predistortion [14] and reduced size LUT [25] show the continued interest in LUT based predistorters. Importantly, this work demonstrates the ability to store sets of coefficients, but determine what set of coefficients to use based on the observed nonlinear performance of the PA, for any given signal. This can avoid the need for the standard LUT approach which has to train a set of coefficients for every possible combination of signal standard and operating power level.

3 Multi-standard Behavioural Modeling

3.1 Data Collection

In order to analyze and study multi-standard behavioural models and implementations, signals were required for each of the standards studied. The signals used were generated in MATLAB using modulation functions from the Communications, LTE & 5G toolboxes. To get the measured results from the PA at different input power levels a testbench was setup, as in Fig. 2 and 3. Here an RFSoC ZCU111 for transmitting and receiving the signals has been used. The signal was generated at the Intermediate Frequency (IF) centred at 1GHz from the RFSoC DAC with sampling frequency of 737.28 MHz and then with the help of the mixer the signal was upconverted to the required center frequency of 2.6 GHz. After this stage, the signal was passed through the GaN-SiC pallet amplifier (RFHIC RTP26010-N1) and the power of the signal was maintained sufficiently to drive the PA in a nonlinear region of operation. This particular PA has two output ports, one of which was connected to a spectrum analyser and the second coupled output port was connected to the downconverter mixer

which uses the same LO frequency as of the upconverter mixer. Here the signal is downconverted back to the IF frequency i.e., 1GHz and is passed to the RFSoC ADC which also has a sampling rate of 737.28 MSPS. In the case of this PA the model memory depth was chosen to be 3 and the non-linear order of the MP model was chosen to be 3.

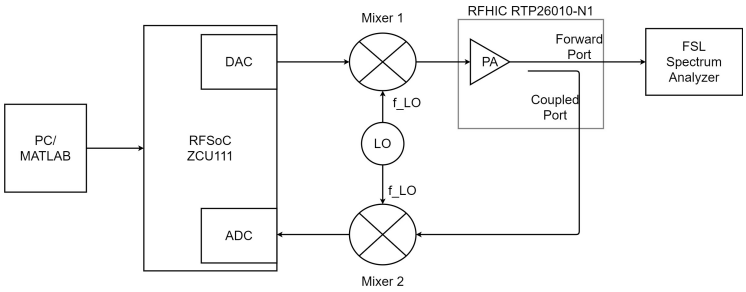

Fig. 2. Test bench block diagram

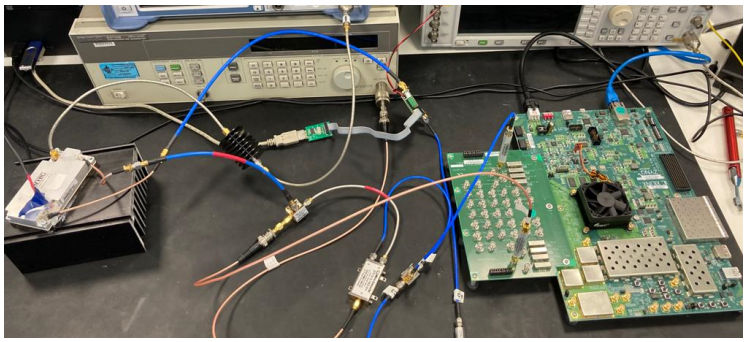

Fig. 3. Experimental Measurement Bench RFSoC ZCU111 with RFHIC RTP26010-N1 PA

For measuring at different power levels, the power of the signals generated from the RFSoC was adjusted using the RF Data Converter Interface. The sample length generated in MATLAB for different standard signals was 70,000 samples. To time align the signal and reduce the noise floor to achieve better dynamic range, the length of the signal captured was 10 times the length of the transmitted signal i.e., 700,000 samples. Once the signal has been time aligned, both the transmitted and received signals were normalised with respect to the maximum absolute value of each. The first 30,000 samples of the averaged input and output signals have been used for training the behavioural model and a further 30,000 were used for the validation of the model.

3.2 AM-AM Distortion Characteristics as Guide to Coefficients

A common technique used to illustrate the characteristic behaviour of a nonlinear power amplifier is the AM/AM curve. The data points from the input and output signals clearly show if the operation of the PA is predominantly linear, when the points populate an approximately straight line, or non-linear when the curve deviates from a straight line. In this work, AM/AM curves are employed to demonstrate the degree to which different signal standards cause different characteristic behaviour from the power amplifier despite the signals having the same average output power level. Fig. 4 shows the discrepancies between experimentally measured 3G, 4G and 5G signals with the same power level (obtained as described in Sec. 3.1), passed through a PA operating nonlinearly.

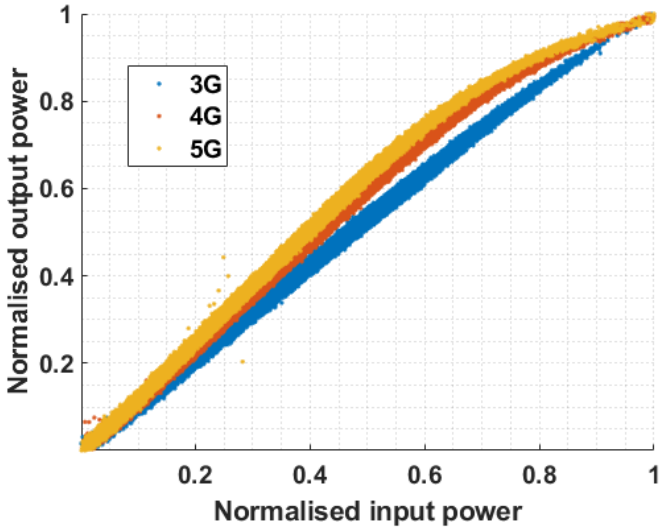

Fig. 4. An experimentally validated illustration of the input-output signal relationship transmitted at 2.6GHz for 3G,4G and 5G signals. Signals were transmitted through the same PA at equivalent transmit power.

Further investigations into PA characterisation given different input signals led to the observation that various AM/AM curves of 3G, 4G and 5G-NR, at different power levels, are very similar, as seen in Fig. 5. Therefore by noting the relative difference in the signal power levels for the different signal standards, that all yield the same characteristic AM/AM performance, one can map the power levels for which the same set of model coefficients can work.

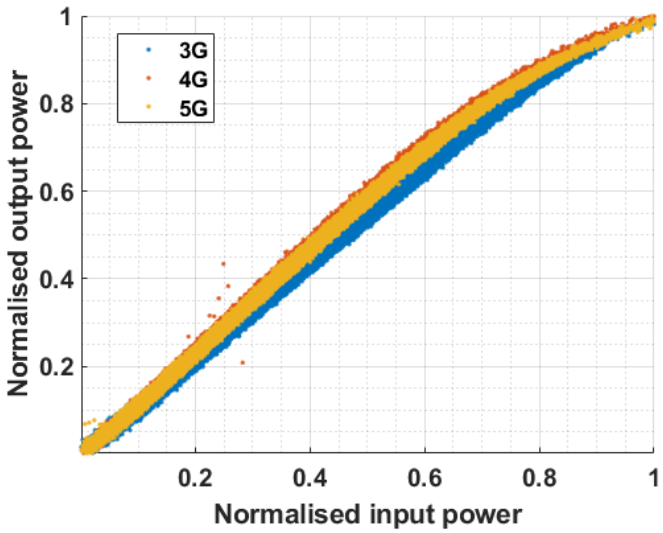

Fig. 5. Experimentally validated AM/AM curve illustrating that 3G, 4G and 5G input signals can produce comparable AM/AM curves given the signals are sent at disparate transmit power levels.

3.3 Multi-Standard Behavioural Models

As indicated in Fig. 4, for the same power amplifier excited by different signals with the same average power level and similar bandwidth, there is a noticeable difference in the AM/AM curves. This in turn indicates a difference of behaviour of the hardware as a result of the different signals. It is therefore not sufficient to assume a particular operating behaviour for the power amplifier based on the average output signal power alone; the signal used must also be taken into account.

This paper presents a means by which a single set of behavioural model coefficients can be extracted and stored in a look-up-table for use with any signal standard so long as the relative power level offsets between different signal types are accounted for. The matching of behavioural model coefficients is implemented across different signal standards. This is performed by extracting coefficients for different power levels for each standard. From the measured output signals the corresponding AM/AM curves are fitted. One set of coefficients are extracted for one signal standard and the AM/AM curve for that standard which best fits the other signal standards is sought.

By exciting the power amplifier using various signals at a range of operating power levels, sets of signals can be compiled and relationships between standards can be learned. Importantly, the signals which match closest in terms of model coefficient performance do not have identical operating power levels.

3.4 Behavioural Model Validation

In order to validate the proposed technique for multiple signal standards, commonly used signal modulation schemes for 3G, 4G and 5G communications are examined. A signal bandwidth of *20 MHz* for single carrier signals were sent through an RFHIC Doherty PA as described in Sec. 3.1.

Table 1. Relationship Between Signal Standards and Power Levels

Coefficient sets	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
5G (dBFS)	**-10**	**-9**	**-8**	**-7**	**-6**	**-5**	**-4**	**-3**
4G (dBFS)	**-18**	**-17**	**-16**	**-15**	**-14**	**-13**	**-12**	**-11**
3G (dBFS)	**-20**	**-19**	**-18**	**-17**	**-16**	**-15**	**-14**	**-13**

Table 2. Cross Signal Standard Model Accuracy NMSE (dB)

	3G MP/GMP	**4G MP/GMP**	**5G MP/GMP**
3G	**-38.386 / -38.39**	**-42.008 / -41.931**	**-41.856/-41.804**
4G	**-42.02/-41.961**	**-45.874 / -45.879**	**-41.995 / -41.918**
5G	**-42.178 / -42.13**	**-39.623/ -30.589**	**-45.874/-44.067**

Pairs of input and output signal datasets are captured for a PA and the AM/AM curves for one signal standard are plotted. A subset of samples from the alternative signal standards at similar power levels are used to check if their AM/AM trace follows a similar trajectory. Comparing these, the relative power levels between standards is determined, and the model coefficients are indexed in the LUT relative to each signal standard power level. The relative power level offsets between standards can be seen in Table 1. In this instance, eight sets of coefficients are matched for the same power amplifier across three different signal standards which each have a relative power level offset.

By knowing the relative power level offsets to use, a behavioral model can be trained for one signal standard and reliably used to model the PA response across the other signal standards. Table 2 illustrates the NMSE comparisons calculated between different signal standards with similar AM/AM curves, which corresponds to one of the columns in Table 1. The columns of Table 2 are populated by training the coefficients using one of the signal standards and validating the model accuracy for all three signal standards. The accuracy for each standard is given in NMSE and placed in its respective row. Independent output signals which were not used to train the models were used for the validation in each case.

4 LUT-based Multi-standard DPD Transceiver

4.1 DPD Coefficient Estimation

The inverse function of the PA system $f(X)$ can be derived by swapping the input signal x and output signal y in Eq. 3. Applying this inverse function f^{-1} will cancel the effect of the PA system f.

$$x_{MP}(n) = \sum_{p=0}^{P} \sum_{m=0}^{M} d_{pm} \hat{y}(n-m)|\hat{y}(n-m)|^p \tag{5}$$

Here $\hat{y}$ is the PA output normalized by PA gain G and with a certain offset T introduced by the PA system.

$$\hat{y} = y(n+T)/G \tag{6}$$

The coefficients d_{pm} of the DPD model can be estimated through different methods. As there are more observations of y and x than the number of coefficients, an over-determined system can be formed. The least squares algorithm is used to estimate the coefficients.

4.2 Hardware Software Co-Design

In Section 3, different standards' signals at different power levels are shown to have the same AM/AM characteristics. Based on this analysis, a Digital Pre Distortion (DPD) solution for transmitting multi-standard signals is implemented, as shown in Fig. 6. This solution shows a way of pre-distorting different standards' signals with sets of coefficients trained by only one signal standard under different power levels. In this way the resource utilization is minimized and associated power consumption of the entire design optimized.

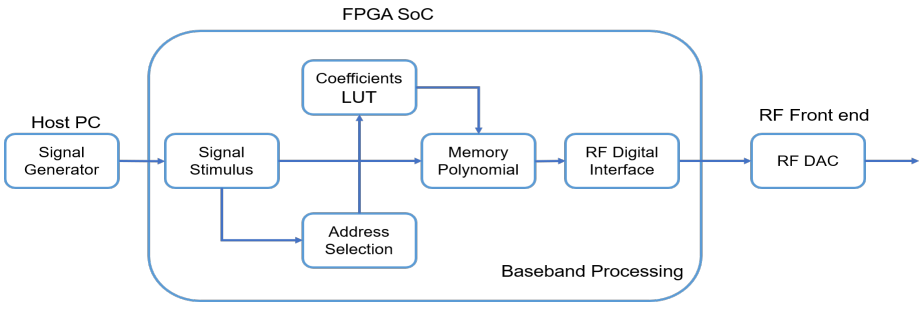

Fig. 6. Proposed System Design Illustration

The proposed design can be divided into two parts: the baseband signal processing and the RF front end. The baseband block handles the predistortion

and other necessary signal processing tasks such as filtering and upsampling. The processed signal is then sent through the RF front end.

On the baseband part, the address selection block is used to calculate the addresses of the coefficients based on the signal power level and standard; these are then sent to the look-up table. The coefficients are loaded from the look-up table to the pre-distorter which, for the PA used in this case, required a memory polynomial model with order 5 and memory depth 5. The resulting pre-distorted baseband signals are then forwarded to the RF front end. For the FPGA implementation, the original input signal in-phase (I) and quadrature (Q) components are used as the input for the pre-distorter block. This pre-distorter block can be updated through the coefficient I/Q ports where I and Q are the real and imaginary parts of the coefficients. In this work, as the RF front end used has 14-bit DACs and ADCs, the interfaces use 16-bit wide AXI buses where the data are transferred as 16-bit fixed point values.

The data interface of the memory polynomial model is AXI-Stream which has 256 bits of data width. It consists of 8 IQ signal pairs, each with 16-bit width. The memory polynomial core will process 8 input signals per clock cycle. To improve the efficiency of the processing, the core utilizes a CORDIC algorithm to calculate the magnitude term in Equation 5.

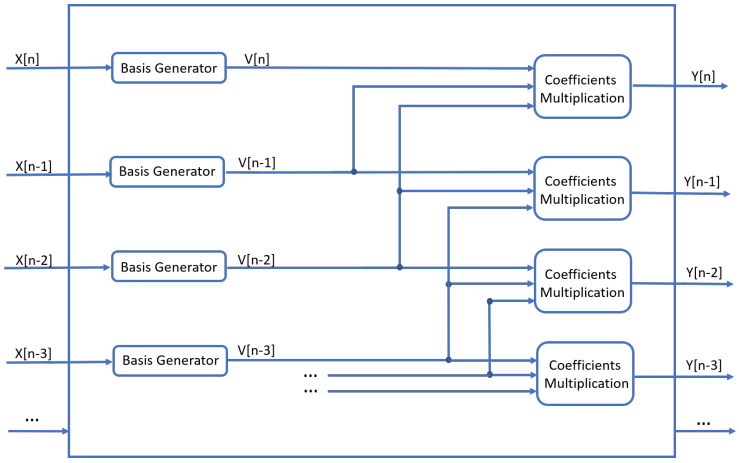

Fig. 7. Parallel Processing Memory Polynomial Hardware Implementation

Implementation details of the parallel memory polynomial model are shown in Fig. 7. The model processes multiple signal samples per clock cycle. The input data is first disassembled into multiple signal samples. Each sample is connected to a basis generation core. This block along with a CORDIC core, calculates the term $x(n)|x(n)|^{p-1}$ and the results are rerouted to the corresponding coefficient multiplication block. Each coefficient multiplication block requires multiple input bases for the memory taps. For simplicity, the figure here illustrates the design

with up to 3 memory taps. In the actual implementation, the memory taps are set to 5. These input bases will be multiplied with the corresponding coefficients. The sum of the results is the output signal.

The addresses selection block requires the transmitted signal as input. The relevant power of the signal is calculated and, along with the chosen signal standard, is used to select the appropriate set of coefficients to use. The update of coefficients is also controlled by this block, where the coefficients are updated constantly.

5 Hardware Implementation and Experimental Validation

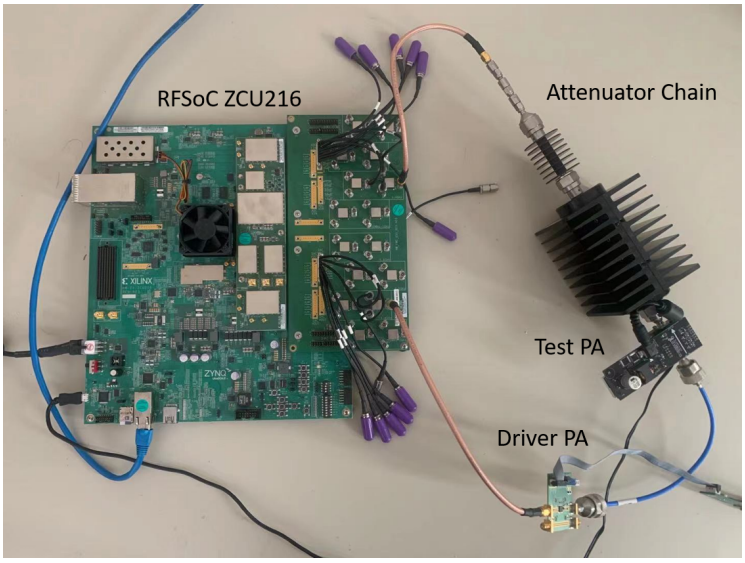

Fig. 8. DPD TestBench RFSoC ZCU216 with NXP's AFSC5G37D37 Doherty PA

The testbench setup is shown in Fig. 8. Xilinx's RFSoC Gen 3 (ZCU216) is used to perform DPD and baseband signal processing. With software and hardware co-design, the address selection block is implemented on the ARM core which utilizes the AXI-Lite bus to update the coefficients based on the input signal. The computationally intensive task of computing the memory polynomial model is performed on FPGA fabric.

The test PA is an AFSC5G37D37 Doherty PA from NXP, which is different from the PA used in the previous validation section. Using a different PA shows the generality of the proposed behaviour modeling and corresponding digital predistortion. Since the output power of the RFSoC is limited, a driver stage

PA BGA7210 is used to increase the input power to the test PA. The BGA7210 is a high linearity PA with variable gain which is operating in its linear region. This PA allows us to set the input signal to different power levels.

5.1 Experiment: DPD performance comparison with different standard's training signals

For these experiments, three DPD models are obtained and each model is trained with a particular signal standard. To validate performance of the resulting DPD coefficients, each set of extracted coefficients are tested for three signal standards, namely 3G, 4G and 5G. From these experiments on the PA hardware, Table 3 shows the NMSE performance for different signal standards. In each row, the test signal is the same, independent of the training model it is applied to. This includes the power level. With the same test signal we achieve similar performance across different standards. The results show that the DPD model can maintain similar performance even when the test signals and training signal are under different standards.

Table 3. NMSE (dB) Comparisons with 3G, 4G and 5G Training and Testing Signal

Test \ Training	3G	4G	5G
3G	-26.36	-25.49	-31.13
4G	-26.80	-31.25	-26.33
5G	-24.88	-24.53	-24.97

5.2 Experiment: DPD performance comparison along different power levels

Exploring in more detail the performance of the proposed technique over different power levels, an experiment is devised where the signals under test are 5MHz 3G signals with different power levels. The different power levels are achieved using the driver PA. The DPD coefficients are trained using 4G signals and to facilitate a direct comparison, the 3G signals. The obtained results are presented in Table 4 and show the NMSE comparison when the input signals are at different power levels. These results show that the proposed DPD has only marginally reduced performance. Additionally, the gap can be narrowed if a greater number of sets of coefficients were trained.

6 Conclusions

This paper provides a definitive solution to behavioural modeling and digital pre-distortion for multiple signal standards. By matching the relative AM/AM

Table 4. NMSE Comparison with 3G Training Signal and 4G Training Signal for 3G Test Signal at Different Power Levels

3G Test Signal Power (dBFs)	-9	-9.5	-10	-10.5	-11	-11.5
4G training signal (dB)	-25.22	-27.59	-28.30	-28.64	-28.91	-30.76
3G training signal (dB)	-28.57	-28.73	-29.86	-29.55	-30.84	-31.94
difference (dB)	-3.35	-1.14	-1.56	-0.91	-1.93	-1.18

curves for different signals passed through the same power amplifier, sets of common coefficients that will work across signal standards can be found. While the technique is demonstrated using polynomial models and Least Squares, the relationships between different input signal standards exist irrespective of the model structure used. Experimental validation is performed using input signals of three different signal modulation schemes, and behavioral modelling and DPD are carried out with experimental measurements using two different PAs from two different manufacturers. The LUT approach works well for both cases and the model or predistorter dimensions can be set in the usual way to cover the characteristic behaviour of the chosen PA. The results show that training of a model, the most computationally intensive aspect, can be done for one signal standard and successfully applied to others provided the relative signal power level offsets are known. Thus the same transmitter design can be used for multiple signal standards.

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